In the Claims:

Claims 1-38 (Cancelled).

39. (Previously Presented) A method for incrementing, decrementing or two's complementing a first string of *N* bits, the method comprising:

generating an auxiliary string of *N* bits as a function of the first string, the auxiliary string having a first least significant bit that is independent from the first string and any other bit of the auxiliary string, and starting from a second least significant bit up to a most significant bit of the auxiliary string, performing a logic combination with a corresponding bit of the first string or a negated replica thereof, starting from a least significant bit up to a second most significant bit of the first string, and of the bits of the first string or the negated replica thereof less significant than the corresponding bit; and

generating an output string as a logic combination of the auxiliary string and of the first string.

40. (Previously Presented) A method according to Claim 39, wherein the least significant bit of the auxiliary string is always null and any other bit, starting from the second least significant bit up to the most significant bit, is a logic OR of a corresponding bit of the first string or of a negated replica thereof and of the bits less significant than the corresponding bit.

41. (Previously Presented) A method according to Claim 39, wherein the least significant bit of the auxiliary string is always 1 and any other bit, starting from the second least significant bit up to the most significant bit, is a logic AND of a corresponding bit of the first string or of a negated replica thereof and of the bits less significant than the corresponding bit.

42. (Previously Presented) A method according to Claim 39, further comprising generating an overflow flag as a logic combination among the most significant bits of the auxiliary string and of the first string.

43. (Previously Presented) A method according to Claim 40, wherein two's complementing the first string comprises obtaining the other bits of the auxiliary string by ORing an immediately less significant bit of the auxiliary string and a corresponding bit of the first string; and wherein generating the output string comprises performing an XOR of the first string to be complemented and the auxiliary string.

44. (Previously Presented) A method according to Claim 41, wherein two's complementing the first string comprises obtaining the other bits of the auxiliary string by ANDing an immediately less significant bit of the auxiliary string and a corresponding bit of the first string; and wherein generating the

output string comprises performing a negated XOR of the first string to be complemented and of the auxiliary string.

45. (Previously Presented) A method according to Claim 40, wherein decrementing the first string comprises obtaining the other bits of the auxiliary string by ORing an immediately less significant bit of the auxiliary string and a corresponding bit of the first string; and wherein generating the output string comprises performing a negated XOR of the first string and of the auxiliary string.

46. (Previously Presented) A method according to Claim 41, wherein decrementing the first string comprises obtaining the other bits of the auxiliary string by ANDing an immediately less significant bit of the auxiliary string and a corresponding bit of the first string; and wherein generating the output string comprises performing an XOR of the first string and of the auxiliary string.

47. (Previously Presented) A method according to Claim 40, wherein incrementing the first string comprises obtaining the other bits of the auxiliary string by ORing an immediately less significant bit of the auxiliary string and the negated replica of a corresponding bit of the first string; and wherein generating the output string comprises performing an XOR of the auxiliary string and a negated replica of the first string.

48. (Previously Presented) A method according to Claim 41, wherein incrementing the first string comprises obtaining the other bits of the auxiliary string by ANDing an immediately less significant bit of the auxiliary string and a corresponding bit of the first string; and wherein generating the output string comprises performing a negated XOR of the first string and of the auxiliary string.

49. (Previously Presented) A method according to Claim 42, wherein the overflow flag is generated by ANDing the most significant bit of the first string and a negated replica of the most significant bit of the auxiliary string when two's complementing or decrementing the first string.

50. (Previously Presented) A method according to Claim 42, wherein the overflow flag is generated by ANDing the negated replicas of the most significant bits of the first string and of the auxiliary string when incrementing the first string.

51. (Previously Presented) A method according to Claim 49, wherein two's complementing the first string with correction of the output string in case of overflow comprises obtaining the other bits of the auxiliary string by ORing an immediately less significant bit of the auxiliary string and a corresponding bit of the string;

the most significant bit of the output string being obtained by NORing the most significant bit of the first string

and the negated replica of the most significant bit of the auxiliary string, any other bit of the output string being obtained by ORing the overflow flag and the logic XOR between corresponding bits of the first string and of the auxiliary string.

52. (Previously Presented) A method according to Claim 49, wherein for two's complementing the first string with correction of the output string in case of overflow comprises obtaining the other bits of the auxiliary string by ORing an immediately less significant bit of the auxiliary string and a corresponding bit of the string;

the most significant bit of the output string being obtained by NORing the most significant bit of the first string and the negated replica of the most significant bit of the auxiliary string, any other bit of the output string being obtained by XORing the overflow flag and the logic XOR between corresponding bits of the first string and of the auxiliary string.

53. (Previously Presented) A method according to Claim 49, wherein decrementing the first string with correction of the output string in case of overflow comprises obtaining the other bits of the auxiliary string by ORing the immediately less significant bit of the auxiliary string and a corresponding bit of the string;

the most significant bit of the output string being

obtained by ORing the most significant bit of the first string and the negated replica of the most significant bit of the auxiliary string, and any other bit of the output string being obtained by XORing the negated replica of the overflow flag and the logic XOR between corresponding bits of the first string and of the auxiliary string.

54. (Previously Presented) A method according to Claim 50, wherein incrementing the first string with correction of the output string in case of overflow comprises obtaining the other bits of the auxiliary string by ORing an immediately less significant bit of the auxiliary string and the negated replica of a corresponding bit of the string;

the most significant bit of the output string being obtained by NORing the most significant bit of the first string and the negated replica of the most significant bit of the auxiliary string, and any other bit of the output string being obtained by ORing the overflow flag and the logic XOR between corresponding bits of the first string and of the auxiliary string.

55. (Previously Presented) A circuit for incrementing, decrementing or two's complementing a first string of *N* bits, the circuit comprising:

an auxiliary circuit for generating an auxiliary string of *N* bits as a function of the first string, the auxiliary string having a first least significant bit that is independent from the

first string and any other bit of the auxiliary string, and starting from a second least significant bit up to a most significant bit of the auxiliary string, said auxiliary circuit performing a logic combination with a corresponding bit of the first string or a negated replica thereof, starting from a least significant bit up to a second most significant bit of the first string, and of the bits of the first string or the negated replica thereof less significant than the corresponding bit; and

logic circuit means for generating an output string as a logic combination of the auxiliary string and of the first string.

56. (Previously Presented) A circuit according to Claim 55, wherein said auxiliary circuit generates the auxiliary string with the first least significant bit always null, with the second least significant bit being a replica of the least significant bit of the first string or as the negated replica thereof, said auxiliary circuit comprising:

N-2 OR gates for generating a respective bit of the auxiliary string, starting from a third least significant bit up to the most significant bit by ORing a corresponding bit of the first string or the negated replica thereof, starting from the least significant bit up to the second most significant bit of the first string, and the bits of the first string or of the negated replica thereof less significant than the corresponding bit.

57. (Previously Presented) A circuit according to Claim 55, wherein said auxiliary circuit generates the auxiliary string with the first least significant bit always null, with the second least significant bit being a replica of the least significant bit of the first string or as the negated replica thereof, said auxiliary circuit comprising:

N-2 OR gates for generating a respective bit of the auxiliary string, starting from a third least significant bit up to the most significant bit, the *N*-2 OR gates being disposed in a cascade of pairs of logic gates, the OR gates of a first pair of logic gates generating the third least significant bit and a fourth least significant bit of the auxiliary string by ORing the second and third least significant bits, respectively, of the first string or of the negated replica thereof, each pair of OR gates being input with a respective pair of consecutive bits of the first string or of the negated replica thereof and the most significant bit of the auxiliary string generated by the pair of gates that precede in the cascade, and generating two consecutive bits of the auxiliary string by ORing the most significant bit generated by the pair of gates that precede in the cascade and respectively a first bit or the respective pair of consecutive bits and both the first bit and a second bit of the respective pair of consecutive bits of the respective pair of bits.

58. (Previously Presented) A circuit according to Claim 55, wherein said auxiliary circuit generates the auxiliary string with the first least significant bit always null, with the

second least significant bit being a replica of the least significant bit of the first string or as the negated replica thereof, said auxiliary circuit comprising:

a cascade of *N*-2 OR gates being input with a respective bit of the first string or of the negated replica thereof in order starting from the second least significant bit up to the second most significant bit of the first string, each OR gate generating a respective bit of the auxiliary string, starting from the third least significant bit up to the most significant bit of the auxiliary string, as a logic OR of the respective bit of the first string or of the negated replica thereof and of the bit of the auxiliary string generated by the OR gate that precedes in the cascade.

59. (Previously Presented) A circuit according to Claim 55, wherein said auxiliary circuit generates the auxiliary string with the first least significant bit always equal to 1, with the second least significant bit being a replica of the least significant bit of the first string or as the negated replica thereof, said auxiliary circuit comprising:

a cascade of *N*-2 AND gates being input with a respective bit of the first string of *N* bits or of the negated replica thereof in order starting from the second least significant bit up to the second most significant bit of the first string, each gate generating a respective bit of the auxiliary string, starting from the third least significant bit up to the most significant bit, by ANDing the respective bit of

the first string or of the negated replica thereof and the bit of the auxiliary string generated by the AND gate that precedes in the cascade.

60. (Previously Presented) A circuit according to Claim 55, further comprising an overflow check circuit for generating an overflow flag as a logic combination among the most significant bits of the auxiliary string and of the first string.

61. (Previously Presented) A circuit according to Claim 58, wherein for two's complementing the first string, each of the bits of the auxiliary string starting from the third least significant bit are obtained by ORing an immediately less significant bit of the auxiliary string and a corresponding bit of the first string; and wherein said logic circuit means comprise:

an array of XOR gates generating bits of the output string by XORing respective bits of the first string to be complemented and of the auxiliary string.

62. (Previously Presented) A circuit according to Claim 58, wherein for decrementing the first string, each of the bits of the auxiliary string starting from the third least significant bit are obtained by ORing an immediately less significant bit of the auxiliary string and a corresponding bit of the first string, and wherein said logic circuit means comprise:

an array of XOR gates, generating bits of a two's complement string by XORing respective bits of the first string to be complemented and of the auxiliary string; and

an array of INVERTER gates each being input with a bit of the two's complement string and generating a corresponding bit of the output string.

63. (Previously Presented) A circuit according to Claim 58, wherein for incrementing the first string, each of the bits of the auxiliary string starting from the third least significant bit are obtained by ORing an immediately less significant bit of the auxiliary string of *N* bits and the negated replica of a corresponding bit of the first string, and wherein said logic circuit means comprise:

an array of XOR gates for generating bits of the output string by XORing respective bits of the first string to be complemented and the auxiliary string.

64. (Previously Presented) A circuit according to Claim 60, wherein for two's complementing or decrementing the first string, said overflow check circuit comprises a logic AND gate for generating the overflow flag, and receives as input the most significant bit of the first string and a negated replica of the most significant bit of the auxiliary string.

65. (Previously Presented) A circuit according to Claim 60, wherein for incrementing the first string, said

overflow check circuit comprises a logic AND gate for generating the overflow flag, and receives as input the negated replicas of the most significant bits of the first string and of the auxiliary string.

66. (Previously Presented) A circuit according to Claim 58, wherein for incrementing or decrementing an input string, the circuit further comprising:

an array of *N* XOR gates each being input with a respective bit of the input string and with a command signal for generating a corresponding bit of the first string, the command signal corresponding to an operation to be performed;

each of the bits of the auxiliary string starting from the third least significant bit being generated by ORing an immediately less significant bit of the auxiliary string and a corresponding bit of the first string; and

said logic circuit means comprising an array of logic gates for generating bits of the output string by XORing a negated replica of the selection command and the logic XOR combination of respective bits of the input string and of the auxiliary string.

67. (Previously Presented) A circuit according to Claim 58, further comprising:

a logic selection circuit receiving as input command signals for identifying an operation to be performed, and for generating first and second selection signals whose logic state

depends on the operation to be performed;

an array of *N* input XOR gates each being input with a respective bit of the input string and with the second selection signal for generating the first string;

each of the bits of the auxiliary string starting from the third least significant bit being obtained by ORing the immediately less significant bit of the auxiliary string and a corresponding bit of the first string; and

said logic circuit means comprising an array of logic gates for generating bits of the output string by XORing the first selection signal and the logic XOR combination of respective bits of the input string and of the auxiliary string.

68. (Previously Presented) A circuit according to Claim 64, wherein for two's complementing with correction of the output string in case of overflow, each of the bits of the auxiliary string starting from the third least significant bit being obtained by ORing an immediately less significant bit of the auxiliary string and a corresponding bit of the first string; and wherein said logic circuit means comprise:

an OR gate being input with the most significant bit of the first string and the negated replica of the most significant bit of the auxiliary string for generating the most significant bit of a two's complement string to be corrected;

an array of XOR gates for generating other bits of the two's complement string to be corrected by XORing corresponding bits of the first string and of the auxiliary string; and

a correction circuit comprising

an INVERTER gate for generating the most significant bit of the output string as a negated replica of the most significant bit of the two's complement string to be corrected, and

an array of *N*-1 OR gates for generating respective other bits of the output string, each gate receiving as inputs the overflow flag and an output of a respective gate XOR of said array of XOR gates.

69. (Previously Presented) A circuit according to Claim 64, wherein for two's complementing or decrementing with correction of the output string in case of overflow, the circuit further comprising:

an input terminal receiving a selection signal of the operation to be performed;

each of the bits of the auxiliary string starting from the third least significant bit being obtained by ORing an immediately less significant bit of the auxiliary string and a corresponding bit of the first string; and wherein said logic circuit means comprise:

an OR gate being input with the most significant bit of the first string and the negated replica of the most significant bit of the auxiliary string for generating the most significant bit of a two's complement string to be corrected;

an array of XOR gates for generating the other bits of the two's complement string to be corrected by XORing

corresponding bits of the first string and of the auxiliary string; and

an output logic circuit being input with the two's complement string, the overflow flag and the selection signal for generating an output bit string equal to the two's complement string, or else the output string is obtained by negating all the bits thereof depending on the logic state of the selection signal and of the overflow flag.

70. (Previously Presented) A circuit according to Claim 69, wherein for two's complementing or decrementing with correction of the output string in case of overflow, said output logic circuit comprising:

a logic correction circuit for generating a negated replica of the selection signal and a correction signal by XORing the selection signal and the overflow flag; and

an array of *N* logic XOR gates, one of said XOR gates m being input with the most significant bit of the two's complement bit string and with the negated replica for generating the most significant bit of the output string, and each other XOR gate being input with a respective other bit of the two's complement string and the correction signal for generating corresponding other bits of the output string.

71. (Previously Presented) A multifunction circuit for decrementing, incrementing or two's complementing an input string of *N* bits, the multifunction circuit comprising:

a logic selection circuit receiving as input command signals for identifying an operation to be performed and for generating first and second selection signals whose logic state depends on the operation to be performed;

an array of *N* XOR input gates each being input with a respective bit of the input string and with the first logic signal, for generating a first string of *N* bits;

an auxiliary circuit for generating an auxiliary string of *N* bits as a function of the first string, the auxiliary string having a first least significant bit that is independent from the first string and any other bit of the auxiliary string, and starting from a second least significant bit up to a most significant bit of the auxiliary string, said auxiliary circuit performing a logic combination with a corresponding bit of the first string or a negated replica thereof, starting from a least significant bit up to a second most significant bit of the first string, and of the bits of the first string or the negated replica thereof less significant than the corresponding bit; and

logic circuit means for generating an output string as a logic combination of the auxiliary string and of the first string, said logic circuit means comprising

an OR gate being input with the most significant bit of the first string and the negated replica of the most significant bit of the auxiliary string for generating the most significant bit of a two's complement string to be corrected,

an array of XOR gates for generating the other

bits of the two's complement string to be corrected by XORing corresponding bits of the first string and of the auxiliary string, and

an output logic circuit being input with the two's complement string, an overflow flag and a first selection signal corresponding to an operation to be performed for generating the output bit string equal to the two's complement string.

72. (Previously Presented) A circuit according to Claim 71, further comprising an overflow check circuit for generating the overflow flag as a logic combination among the most significant bits of the auxiliary string and of the first string.

73. (Previously Presented) A circuit according to Claim 72, wherein said overflow check circuit comprises a logic AND gate for generating the overflow flag, and receives as input the most significant bit of the first string and a negated replica of the most significant bit of the auxiliary string.

74. (Previously Presented) A multifunction circuit according to Claim 71, wherein said logic selection circuit receives as input first and second command signals for generating the first selection signal by NORing the first and second command signals, and a second selection signal by ANDing the first command signal and a negated replica of the second command

signal.